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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/622,734	11/27/2000	Keisuke Koga	YAO-432US	2803

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EXAMINER	
MONDT, JOHANNES P	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 02/24/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/622,734	KOGA, KEISUKE	
	Examiner	Art Unit	
	Johannes P Mondt	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 October 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7 and 9-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-3,7,9-14 and 17-22* is/are allowed.

6)☒ Claim(s) *4-6,14 and 15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

Amendment filed 10/02/03 forms the basis of this Official Action. No claims have been either added, cancelled or amended. Comments on Remarks in said Amendment are included below under "Response to Arguments".

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. ***Claims 4 and 15*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Kuriyama et al (5,550,435) in view of Kojima (5,965,921) and Kawaguchi (JP401061953A) (as listed in the Information Disclosure Statement of Paper No. 5).

With regard to claim 4: Kuriyama et al teach (cf. Figure 3) a field emission type electron source device (cf. title and abstract) comprising:

a field emission electron source portion including an extraction electrode 2 (cf. column 4, line 38) provided on a p-type silicon substrate 5 (cf. column 4,

line 39) via an insulating film 3 (cf. column 4, line 38) and having an opening portion (located around 1, see Figure 3) at a position corresponding to a region where a cathode is provided; and a cathode portion provided on the p-type silicon substrate and at a position corresponding to the opening portion of the extraction electrode; and

an n-channel field effect transistor portion (comprising IGFET gate 8, channel between source 6 and drain 4/6; cf. column 4, line 41) provided on the p-type silicon substrate, corresponding to the field emission electron source portion, wherein:

the field emission electron source portion is provided in a drain region 4/6 (cf. column 4, lines 39-40) of the field effect transistor portion; and a control voltage is applied to a gate electrode 8 (cf. column 4, line 41) of the field effect transistor portion to control a field emission current from the field emission source portion., while part of the aforementioned gate electrode 8 covers the drain region 4 (cf. Figure 3).

Kuriyama et al do not necessarily teach the further limitation that the gate electrode of the field effect transistor portion has a shape such that a portion of the gate electrode nearer the drain region has a total width wider than a total width of a portion of near the source region. However, in order to prevent hot carrier generation in a depletion layer of the drain junction, Kawaguchi teaches a gate electrode 1 in a MOS transistor to be wider on the drain side 2 than on the source side 3 (see "Purpose" and "Constitution" in Abstract).

Motivation to include the teaching of Kawaguchi in this regard in the invention by Kuriyama et al stems from the circumstance that suppression of said hot carrier generation would increase the withstand voltage in any MOSFET, irregardless of whether said MOSFET is incorporated into a field emission cathode apparatus of the type essentially taught by Kuriyama et al, while an attempt to achieve an overall increase the withstand voltage is in line with the objective of Kuriyama et al (see column 1, line 55 – column 2, line 11).

Furthermore, all that is necessary for a *combination* of the inventions is a widening of the gate near the drain. Therefore, *reasonable expectation of success* is justified.

The extraction electrode as taught by Kuriyama et al is provided in a region above the drain region and away from an interface between regions of different impurity concentrations, namely the region in the upper right corner of Figure 3 marked "Grid Electrode").

3. ***Claims 5 and 16*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Kuriyama et al (5,550,435) in view of Kojima (5,965,921). Kuriyama et al teach (cf. Figure 3) a field emission type electron source device (cf. title and abstract) comprising:

a field emission electron source portion including an extraction electrode 2 (cf. column 4, line 38) provided on a p-type silicon substrate 5 (cf. column 4, line 39) via an insulating film 3 (cf. column 4, line 38) and having an opening portion (located around 1, see Figure 3) at a position corresponding to a region

where a cathode is provided; and a cathode portion provided on the p-type silicon substrate and at a position corresponding to the opening portion of the extraction electrode 2; and

an n-channel field effect transistor portion (comprising IGFET gate electrode 8, channel between source 6 and drain 4/6; cf. column 4, line 41) provided on the p-type silicon substrate, corresponding to the field emission electron source portion, wherein:

the field emission electron source portion is provided in a drain region 4/6 (cf. column 4, lines 39-40) of the field effect transistor portion; and a control voltage is applied to a gate electrode 8 (cf. column 4, line 41) of the field effect transistor portion to control a field emission current from the field emission source portion;

the drain region includes at least two wells 4 and 6 having different impurity concentrations (4 is n-doped and 6 is n+ doped silicon) (cf. column 4, lines 45-46); and

of the at least two wells, one well having a low impurity concentration is provided at an end of the drain (said drain being to the left of the channel between drain and source; cf, Figure 3) which contacts the channel region of the field effect transistor portion.

Kuriyama et al do not necessarily teach the further limitation that the well having low impurity concentration is provided around a circumference of the other well having a higher impurity concentration. However, as is evidenced by Kojima, it is well known in

the art of field effect transistors with insulated gate that the rated voltage can be improved by surrounding the heavily doped drain region by a lightly doped drain region so as to further reduce the gate-drain capacitance; see column 9, lines 1-40 and column 11, line 54 – column 12, line 8). The relevant component in Kuriyama is indeed a field effect transistor with insulated gate, and hence the art is analogous.

Motivation to include the teaching by Kojima in this regard is the desirability to improve the rated voltage for any insulated gate field effect transistor, including the IGFET in the invention by Kuriyama et al. The inventions can be easily combined through slightly extending the lightly doped drain region. Success in implementing the combination of the teaching by Kojima and the invention by Kuriyama et al can therefore be reasonably expected.

The gate insulation film between the p-silicon substrate 5 and IGFET gate 8 as taught by Kuriyama et al is thinner than the first insulating film 3 (see Figure 3) while the first insulating film is provided between the extraction electrode 2 and the p-type silicon substrate 5. Thus, it is concluded that claim 5 is unpatentable over Kuriyama et al in view of Kojima.

With regard to claim 16: the extraction electrode 2 as taught by Kuriyama et al is provided in a region above the drain region and away from an interface between regions of different impurity concentrations, namely the region in the upper right corner of Figure 3 marked "Grid Electrode". Therefore, the further limitations as defined by claims 14 and 16 do not distinguish over the primary reference (Kuriyama et al).

1. ***Claim 6*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Kuriyama et al and Kojima as applied to claim 5 above, and further in view of Hirano et al (JP409063467A).

As detailed above, Kuriyama et al anticipate Claim 5; however, they do not necessarily teach the further limitation of Claim 6. Nevertheless, it would have been obvious to use thermal oxidation to produce the insulating film as it is understood in the art that silicon dioxide is an excellent insulating film generally in semiconductor field effect device technology while it is economically produced, given the silicon substrate suitable to provide the fuel, while *Hirano et al teach the use of thermal oxidation of silicon* for the more specific purpose of sharpening the tip of the cathode portion of the field emission electrode source portion of their cold cathode device; see [0034] and title and abstract. *Motivation* to combine stems from the requirement of a micropoint of the electron emitter taught by Kuriyama et al; see their claim 1 for instance. *Combinability* of the inventions by Kuriyama et al and Hirano et al is obvious in view of the efficiency of producing said tip and gate insulating film together in this manner. *Reasonable expectation of success* of the combination of said inventions follows from the fact that no new steps are introduced at any stage.

Allowable Subject Matter

4. ***Claims 1-3 and 14*** are allowed. The following is a statement of reasons for the indication of allowable subject matter:

Kojima specifically teaches that "the source region to be symmetrical in structure with its associated drain region" (column 12, lines 19-27). Motivation to include the teaching by Kojima in the invention by Kuriyama is provided by the analogue of the intermediate gate electrode 105 (column 9, line 4) in the form of extraction electrode 2: reduction of the influence of the capacitance between said extraction electrode 2 in Kuriyama, - corresponding to the intermediate gate electrode 105 in Kojima, and the corresponding drain 103 is the primary motivation (see column 12, lines 19-27). However, it does not necessarily follow from the above that within the drain region itself both wells must have *"impurity concentrations having symmetrical impurity distributions", because the symmetry taught literally by Kojima is confined to inter-source-drain symmetry, not intra-drain symmetry*. The rejection of claim 1 and dependent claims is therefore withdrawn. After an update of the search, taking into account the broader language of the currently amended claim 1, claims 1-3 and 14 (dependent upon claim 1) are herewith indicated as allowed.

2. ***Claims 7 and 17*** are allowed.

3. The following is a statement of reasons for the indication of allowable subject matter: Shielding electrodes in the art of field emission type electron sources with field effect transistor and made of the same material as the gate electrode, are known in the prior art as witnessed by *Ishikawa et al (JP60124872)*. However, although this teaching would be pertinent to the MOSFET aspect of the invention by Kuriyama et al, said

shielding electrode by Ishikawa et al (a) is not held at the same potential as the substrate, and (b) is neither shown nor described to cover a region of the channel. Shielding electrodes with the additional two features (a) and (b) described above have not been found in the Prior Art to date, nor has any reason surfaced as to why such shielding electrodes should be obvious.

4. ***Claims 9-13 and 18-22*** are allowed. The following is a statement of reasons for the indication of allowable subject matter: Although the first portion of claim 9 is taught by Kuriyama, i.e., up to and including line 14 on page 67 of the claim as printed in the disclosure, Kuriyama et al do not teach the further limitation for the drain region (lines 15-18), nor the further limitation for the gate electrode (lines 19-22), the latter with the exception that the gate electrode 8 is positioned lower than the extraction electrode 2, which is taught by Kuriyama et al (see discussion of claim 1). Although Shimomura et al is valid art under 102(a) unless the earliest of the two foreign priority documents is perfected, and although Shimomura et al teach within the context of a MOSFET that the drain 2 should be surrounded by the source region 3 (Figure 1 and page 9, Embodiment 1), and although the teaching by Shimomura et al further includes a symmetrical placement of the gate with respect to the *drain*, both teachings being motivated by the reduction of electric noise through fluctuations particularly for high-frequency applications (cf. abstract and page 6, line 57 – page 7, line 19 and page 8, lines 5-19), no teaching of a similar nature with regard to a symmetrical placement of the gate with respect to the emission cathode in a field effect device is available. The same comment

applies to claim 18, which is taught by Kuriyama et al up to and including line 14 on page 5 of Amendment C, while, with the exception of the teaching by Kuriyama et al of the positioning of the gate electrode at a location lower than the extraction electrode, the further limitations on the drain region of the field effect transistor portion and on the gate electrode of the field effect transistor portion are identical to those in claim 9, and hence the same comment applies to the close but incomplete teaching by Shimomura et al in this regard.

Response to Arguments

1. Applicant's arguments filed 10/02/03 have been fully considered but they are not persuasive.

With regard to "Allowable Subject Matter", indeed, with "allowable" was meant "allowed".

With regard to the text on the traverse of the rejections under 35 USC 103(a) of claims 4 and 15, the phrase in bold "a part f the gate electr de is provided in such a manner as to cover an end f the drain regi n" on pages 2 and 3 of "Remarks / Arguments" will be interpreted in what follows to mean "a part of the drain electrode is provided in such a manner as to cover an end of the drain region".

Applicant alleges that n-type ("silicon channel" region 4 is not and cannot be part of the drain region" (page 3 of Remarks) is not accepted. In particular, lightly doped region 4 in Kuriyama is of the same conductivity type as the abutting highly doped drain region 3 and therefore is what is known as a lightly doped drain (LDD) region. Applicant's own disclosure of the feature in claim 4 that "a part of the gate electrode is

provided in such a manner as to cover an end of the drain region" in no way distinguishes from Kuriyama in this respect, because in none of the Drawings in the Specification does the gate electrode overlap the heavily doped portion 3 of the drain, instead only overlapping the source and the lightly doped portion of the drain. Specifically,

(a) Figure 1, where gate electrode 8 overlaps with 4 (cf. page 26 of the Specification, particularly the following text on lines 9-11: "4, a third n-type semiconductor conductive portion with a low impurity concentration which is a drain region of the FET") and with 2 (source, not drain; see page 26, lines 5-7), but not with 3, i.e., (see page 26, lines 8-9) "the second n-type semiconductor conductive portion with a high impurity concentration which is a drain region of the FET".

(b) Figure 2, where gate electrode 8T overlaps with 2 and 4 but not with 4: see page 27 of the Specification, in particular the text "the n-type semiconductor conductive portions 3 and 4 serving as a drain" (lines 12-13);

(c) Figure 3, wherein gate electrode 39 (page 32, line 15) overlaps 32 (source) and 34 (lightly doped drain) and but not 33 (heavily doped drain): see the following text: "32, a first n-type semiconductor conductive portion which is a source region of an element operating as a field effect transistor (FET); 33, a second n-type semiconductor portion with a high impurity concentration which is a drain region of the FET; 34, a third n-type semiconductor conductive portion with a low impurity concentration which is a drain region of the FET" (page 31, final line – page 32, line 8);

(d) Figure 4, wherein gate electrode 49 (page 37, line 31) overlaps regions 42 (source; cf. page 37, line 14-15) and region 44 (44 serves as a drain region, see page 36, lines 30-32) but not region 43 (high concentration impurity region serving as drain; cf. page 36, lines 28-30);

(e) not overlap is in evidence form Figures 5-7;

(f) Figure 8 is a Prior Art Figure.

Second, Applicant's traverse that in the Kuriyama Patent "the electric current flow is in the opposite direction of the flow of electrons in applicant's claimed invention" (page 3 of Remarks) does not distinguish said Patent from Applicant's invention, because electric current flow and electron flow are inherently opposite to each other by virtue of the negative elementary charge of the electron.

With regard to the comment on Kojima and Kawaguchi: as, in view of the above, nothing needs rectification in what Kuriyama has been stated to teach, said comment is moot.

Therefore, the traverse of the rejections of claims 4 and 15 cannot be accepted.

With regard to the text on the traverse of the rejection under 35 USC 103(a) of claims 5 and 16, Applicant's traverse appears to be based on an alleged failure to teach the gate insulation film and the first insulation film as different films such that the gate insulation film is thinner than said first insulation film. However, "thickness" exclusively pertains to the vertical direction, while it is evident from Figure 3 as cited in the rejection that the gate insulation film is at least thinner than said first insulation film ("Insulator Layer 3") by an amount equal to the thickness of the gate 8 and furthermore, that said

gate insulation film is at least distinct from said first insulation film in view of the three separate portions of fist insulation film shown in Figure 3. Moreover, the gate insulation film by definition is the insulator that insulates the gate from the channel, and hence only the lower portion sandwiched between the gate 8 and the channel between regions 4 and 6 (lightly doped drain and source) qualifies properly as "gate insulation film". Note in this regard that the Specification of Applicant also defines the gate insulation film to be the gate insulation of the field effect transistor (FET) (see page 20, lines 30-31). FET gate insulation film thickness in standard terminology is defined as the thickness of the layer between the gate and the channel. See, for instance S.M. Sze, "Physics of Semiconductor Devices", Chapter 8, pp. 433-434, particularly Figure 3 (for a full reference see PTO Form 892). The secondary reference Kojima appears to be traversed only for not making up for the deficiency of Kuriyama in the above respect (page 5 of Remarks).

Applicant also appears to base his traverse on the contiguity of insulation film and first insulation film; however, three separate regions 3 exist and the gate insulation film resides in only one of them. Furthermore, non-contiguity has not been claimed.

Therefore, the traverse of the rejection of independent claim 5 and claim 15 dependent thereon, for which claim 15 no independent arguments of traverse have been submitted, cannot be accepted.

*With regard to the text on the traverse of the rejection under 35 USC 103(a) of claim 6,*Applicant's traverse merely states that Hirano, i.e., the additional reference, does not appear to rectify "the deficiencies heretofore discussed with respect to the

Kuriyama and Kojima references". Therefore, in view of the above arguments explaining why no such deficiencies exist, the traverse of the rejection of claim 6 cannot be accepted.

Conclusion

2. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Johannes P Mondt whose telephone number is 571-272-1919. The examiner can normally be reached on 8:00 - 18:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on 571-272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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SUPERVISORY PATENT EXAMINER
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JPM
February 15, 2004